

2814



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes et al.

Title: DEAPROM AND TRANSISTOR WITH GALLIUM NITRIDE OR GALLIUM ALUMINUM NITRIDE GATE

Docket No.: 303.355US4

Serial No.: 09/883,795

Filed: June 18, 2001

Due Date: March 12, 2002

Examiner: Theresa T. Doan

Group Art Unit: 2814

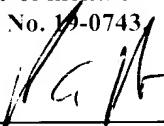
Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

A return postcard.
 An Amendment and Response under 37 CFR § 1.111 (9 Pages).
 Clean Version of Amended Specification Paragraphs (4 pgs.).
 Reference: In re Sang Su Lee, 00-1158 (Fed. Cir. 2002) (14pgs).

Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and
please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this 12th day of March, 2002.

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(GENERAL)

S/N 09/883,795

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DEAPROM AND TRANSISTOR WITH GALLIUM NITRIDE OR GALLIUM
ALUMINUM NITRIDE GATE

Commissioner for Patents
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Applicant has reviewed the Office Action mailed on December 12, 2001. Please amend the above-identified patent application as follows.

IN THE SPECIFICATION

Delete lines 6-18 on page 1 of the originally filed application, beginning with the heading "Cross Reference To Related Applications".

Please make the paragraph substitutions indicated in the appendix entitled Clean Version of Amended Specification Paragraphs. The specific changes incorporated in the substitute paragraphs are shown in the following marked-up versions of the original paragraphs:

The paragraph beginning at page 8, line 23 is amended as follows:

Figure 1 is a simplified schematic block diagram illustrating generally one embodiment of a memory **100** according to one aspect of the present invention, in which reduced barrier energy floating electrode memory cells are incorporated. Memory **100** is referred to as a dynamic electrically alterable programmable read only memory (DEAPROM) in this application, but it is understood that memory **100** possesses certain characteristics that are similar to DRAMs and flash EEPROMs, as explained below. For a general description of how a flash EEPROM operates, see B. Dipert et al., "Flash Memory Goes Mainstream," IEEE Spectrum, pp. 48-52 (Oct. 1993), which is incorporated herein by reference. Memory **100** includes a memory array **105** of multiple memory cells **110**. Row decoder **115** and column decoder **120** decode addresses provided on address lines **125** to access the addressed memory cells in memory array **105**.